REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-10 and 26-44 are in this application. Claims 1, 2, and 5-10 have been amended. Claims 11-25 have been cancelled. Claims 26-44 have been added to alternately and additionally claim the present invention.

The title of the invention has been amended to more accurately describe the invention.

The Examiner restricted the invention to claims 1-10 and 22-23 which are drawn to a device, or claims 11-21 and 24-25 which are drawn to a method of forming the device. On May 22, 2002, applicant's attorney provisionally elected to prosecute claims 1-10 and 22-23, and hereby affirms that election.

The Examiner rejected claim 4 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art ... to make and/or use the invention. Specifically, the Examiner argued that the limitation "wherein the bottom surface has multiple levels" is not supported by the specification.

Applicant directs the Examiner to the first full paragraph on page 10 of applicant's specification (lines 6-11), which reads as follows:

> "The top metal layer, metal-4 layer 344 in this example, functions as a mask for the etching step, with the remaining layers of metal functioning as an etch stop. Thus, depending on the metal patterns in interconnect 300, the bottom surface of a trench TR can have multiple levels, such as trench TR2 (which steps up and over patterned metal-2 layer 324), or a single level such as trench TRs."

Thus, the limitation "wherein the bottom surface has multiple levels" appears to be supported by the specification. As a result, claim 4 satisfies the requirements of the first paragraph of section 112.

The Examiner also rejected claims 5, 22, and 23 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the examiner noted that the limitations referencing trenches in claims 5, 22, and 23 lacked antecedent basis.

Claim 5 has been amended to depend from claim 2, rather than claim 1 (claims 22-23 have been cancelled). For the same reason, claims 8 and 9 have also been amended to depend from claim 2. As a result, claims 5, 8, and 9 are believed to comply with the requirements of 35 U.S.C. §112, second paragraph.

The Examiner rejected claims 1-5, 7-9, and 22-23 under 35 U.S.C. §102(b) as being anticipated by Koo et al. (U.S. Patent No. 6,262,446). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 1 has been amended and recites, in part,

> "a dielectric structure formed between laterally adjacent metal lines of a patterned metal layer, the dielectric structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material."

(Claim 1 has also been amended to further clarify the claim.)

In rejecting claim 1, the Examiner pointed to capacitor 20 shown in FIG. 4 of Koo as constituting the dielectric structure required by claim 1. The Koo reference, however, does not teach that dielectric layer 17a of capacitor 20 is formed between laterally adjacent metal lines of a patterned metal layer as required by amended claim 1.

As shown in FIG. 4, Koo teaches that dielectric layer 17a is formed between vertically adjacent metal regions that are formed from two metal layers. Thus, since Koo fails to teach that dielectric layer 17a is formed between laterally adjacent metal lines, claim 1 is not anticipated by Koo. In addition, since claims 2-5 and 7-9 depend either directly or indirectly from claim 1, claims 2-5 and 7-9 and are not anticipated by Koo for the same reasons as claim 1.

Regarding claim 2, the Examiner appears to point to the via openings that are formed between interconnection 36b and capacitor 21 as constituting a trench of the trenches required by claim 2. Koo discloses, however, that these via openings are filled with a conductive material. (See col. 6, lines 20-25 and 35-39.)

Claim 2 has been amended to recite, in part,

> "a plurality of trenches formed in the layers of insulation material, each trench adjoining metal lines of the top patterned metal layer, a trench extending from the top metal layer between metal lines of the top metal layer through the top insulation layer and between metal lines of a metal layer lying below the top metal layer, each trench having a bottom surface, the trenches not including a conductive material."

Thus, since the Koo reference does not appear to teach trenches that do not include a conductive material, claim 2 is patentable over Koo et al for this additional reason.

The Examiner objected to claims 6 and 10 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 6 and 10 have been rewritten as independent claims and are believed to incorporate all of the limitations of the base claim. (Claim 10 also includes a reference to a plurality of trenches.)

New claim 26 recites,

> "a first plurality of metal lines that lie in substantially a same horizontal plane, the first plurality of metal lines including first, second, and third metal lines, the first, second, and third metal lines each having a top surface, a bottom surface, and side wall surfaces that contact the top and bottom surfaces;
>
> "a first dielectric that contacts the first metal line and the second metal line; and
>
> "a second dielectric that contacts the second metal line and the third metal line, the second dielectric being different from the first dielectric."

However, as shown in FIG. 4 of Koo, dielectric layer 17a can not be read to be the second dielectric because dielectric layer 17a does not contact two metal lines that lie in substantially a same horizontal plane. Thus, claim 26 is not anticipated by the Koo reference. In addition, since new claims 27-37 depend either directly or indirectly from claim 26, claims 27-37 are not anticipated by Koo for the same reasons as claim 26.

New claim 38 recites,

> "a first plurality of metal lines that lie in substantially a same horizontal plane, the first plurality of metal lines including first, second, and third metal lines, the first, second, and third metal lines each having a top surface, a bottom surface, and side wall surfaces that contact the top and bottom surfaces;
>
> "a first dielectric that contacts the first metal line and the second metal line; and
>
> "a second dielectric that contacts the side wall of the third metal line, the second dielectric being different from the first dielectric."

As shown in FIG. 4 of Koo, dielectric layer 17a can not be read to be the second dielectric because dielectric layer 17a does not contact the side wall of any of the metal lines. Thus, claim 38 is not anticipated by the Koo reference. In addition, since new claims 39-44 depend either directly or indirectly from claim 38, claims 39-44 are not anticipated by Koo for the same reasons as claim 38.

Thus, for the foregoing reasons, it is submitted that the specification and all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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APPENDIX

In the Title

Please amend the title in all instances as follows:

MULTILEVEL METAL INTERCONNECT [AND METHOD OF FORMING THE INTERCONNECT] WITH CAPACITIVE STRUCTURES THAT ADJUST THE CAPACITANCE OF THE INTERCONNECT

In the Claims

Please cancel claims 11-25.

Please amend the claims as follows:

1. (Amended) A multilevel metal interconnect formed on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, a patterned metal layer including a plurality of metal lines, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers; and

a [capacitive] dielectric structure formed between laterally adjacent metal lines of a patterned metal layer, the [capacitive] dielectric structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material.

2. (Amended) The multilevel metal interconnect of claim 1 and further comprising a plurality of trenches formed in the layers of insulation material, each trench adjoining metal lines of the top patterned metal layer, a trench extending from the top metal layer between metal lines of the top metal layer through the top insulation layer and between metal lines of a metal layer lying below the top metal layer, each trench having a bottom surface, the trenches not including conductive material.

5. (Amended) The multilevel metal interconnect of claim [1] 2 wherein the bottom surface of the trench is spaced apart from a top surface of the semiconductor substrate.

6. (Amended) [The multilevel metal interconnect of claim 1 wherein] A multilevel metal interconnect formed on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers; and

a capacitive structure formed between adjacent metal lines of a patterned metal layer, the capacitive structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material, the dielectric material [includes] including a plurality of layers of dielectric material.

7. (Amended) The multilevel metal interconnect of claim 1 wherein the [capacitive] dielectric structure has a layer of material formed to adjoin a layer of insulation material, the layer of material being different from the layer of insulation material.

8. (Amended) The multilevel metal interconnect of claim [1] 2 wherein the [capacitive] dielectric structure is formed adjacent to a trench.

9. (Amended) The multilevel metal interconnect of claim [1] 2 wherein the [capacitive] dielectric structure is formed between a pair of adjacent trenches.

10. (Amended) [The multilevel metal interconnect of claim 1 wherein] A multilevel metal interconnect formed on a semiconductor substrate, the

semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers;

a capacitive structure formed between adjacent metal lines of a patterned metal layer, the capacitive structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material; and

a plurality of trenches formed in the layers of insulation material, a first trench [is] being filled with air and a second trench [is] being filled with the capacitive structure.

New claims 26-44 have been added.